

FIG. 1 is a block diagram of a mobile communications system 100. The system 100 includes a mobile communications network 104, which is connected to a controller unit 108. The network 104 is also connected to two base stations, 102A and 102B. Base station 102A is connected to two mobile devices, 106X and 106Y. Base station 102B is connected to one mobile device, 106Z. The mobile devices 106X, 106Y, and 106Z are shown as mobile phones. The network 104 is represented by a cloud shape. The controller unit 108 is represented by a rectangle. The base stations 102A and 102B are represented by towers. The mobile devices 106X, 106Y, and 106Z are represented by mobile phones. The system 100 is shown in a cross-section view.

100 ↗

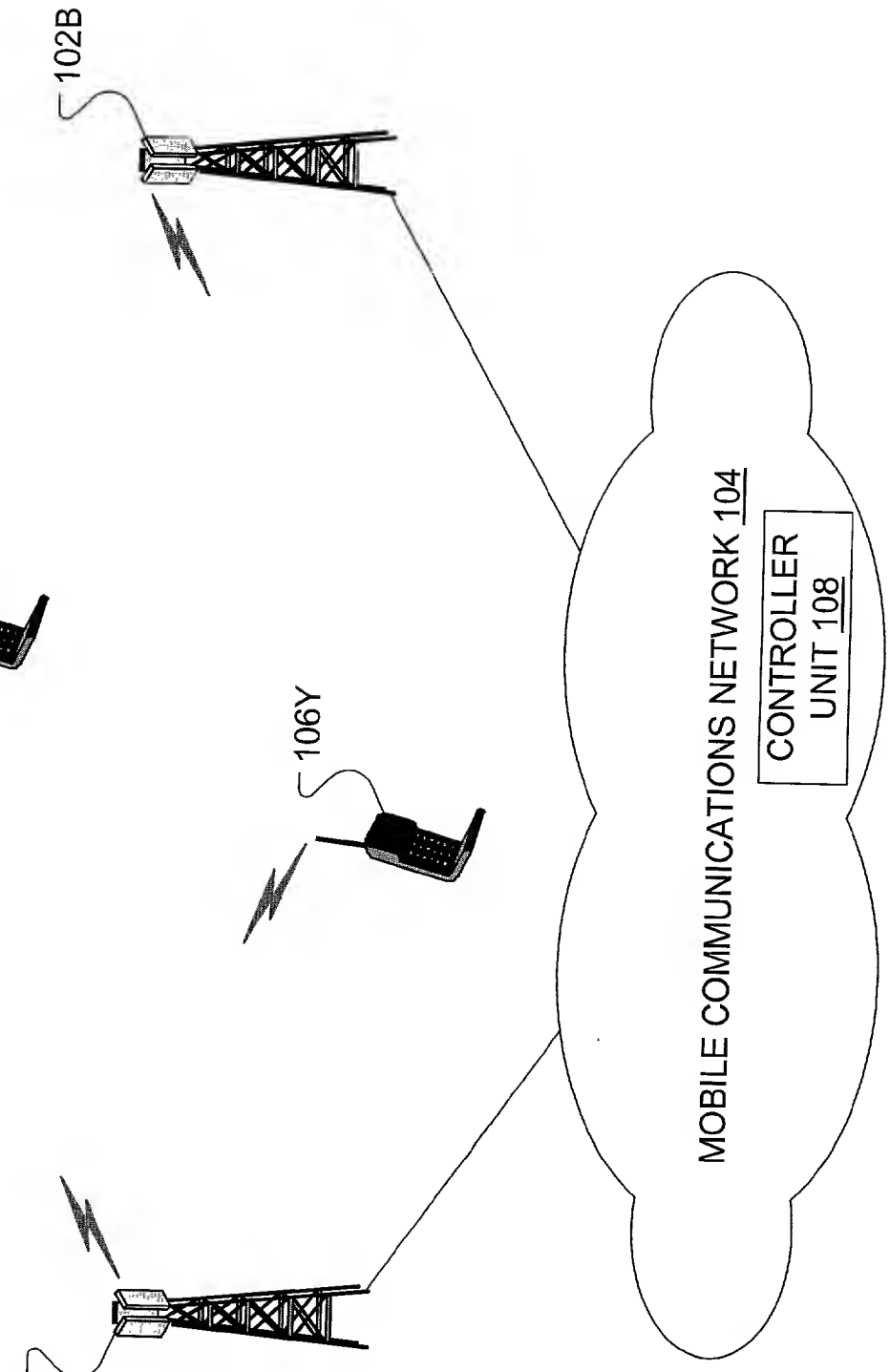


FIG. 1

FIG. 2 is a diagram illustrating a sub-carrier frequency band and sub-carrier frequency for a transmitter and receiver. The diagram shows a channel frequency band (202) and a sub-carrier frequency (204) for a transmitter and receiver. The transmitter side shows sub-carriers 1 through N-7, followed by an ellipsis, and then sub-carriers 11, 9, 7, 5, 3, and 1. The receiver side shows sub-carriers 2, 4, 6, 8, 10, and 12, followed by an ellipsis, and then sub-carriers N-6, N-4, N-2, and N. The sub-carrier amplitude is indicated by the height of the peaks.

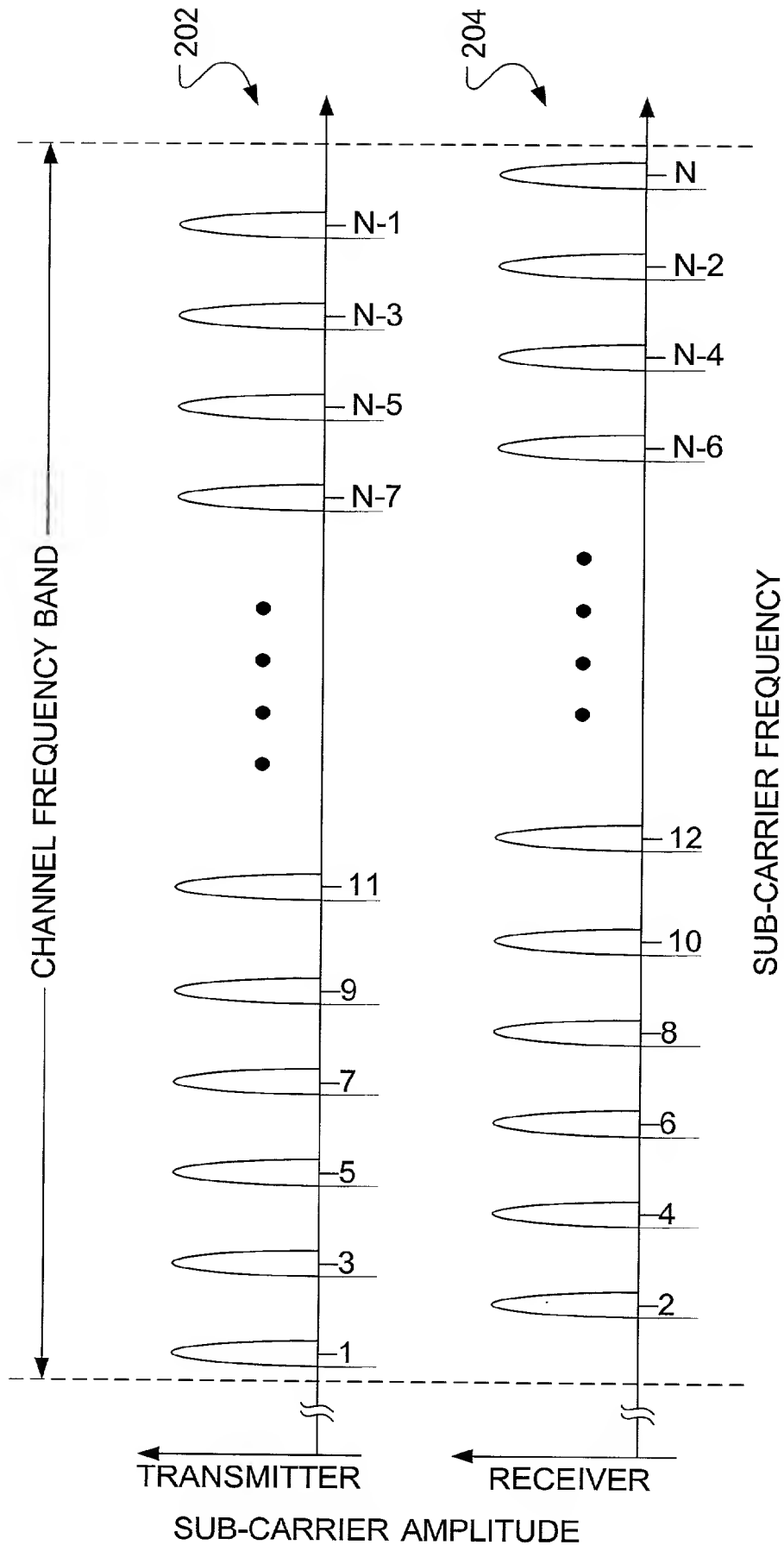


FIG. 2

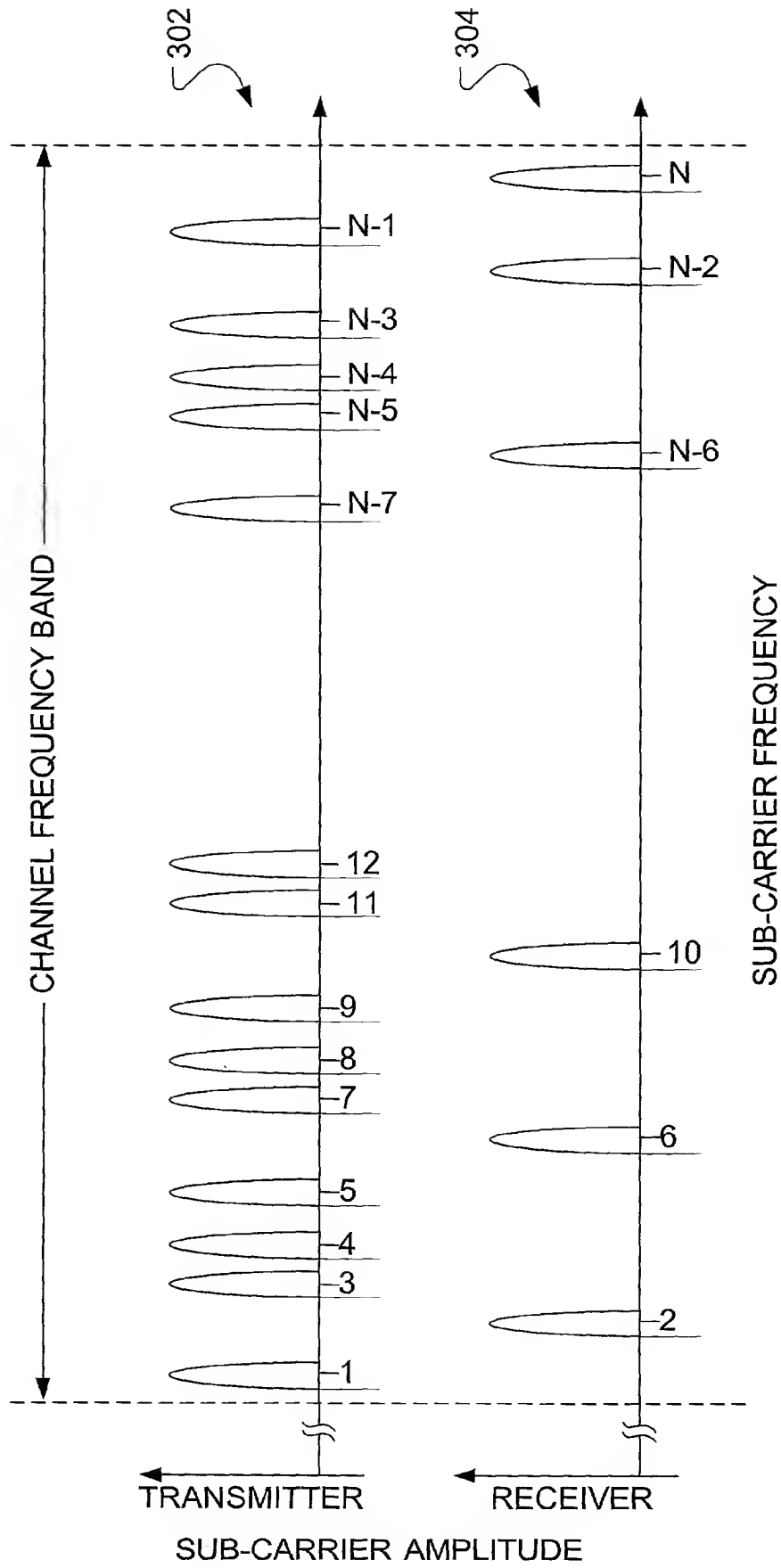


FIG. 3

FIG. 4 is a block diagram of a communication system 400, according to one embodiment of the present invention.

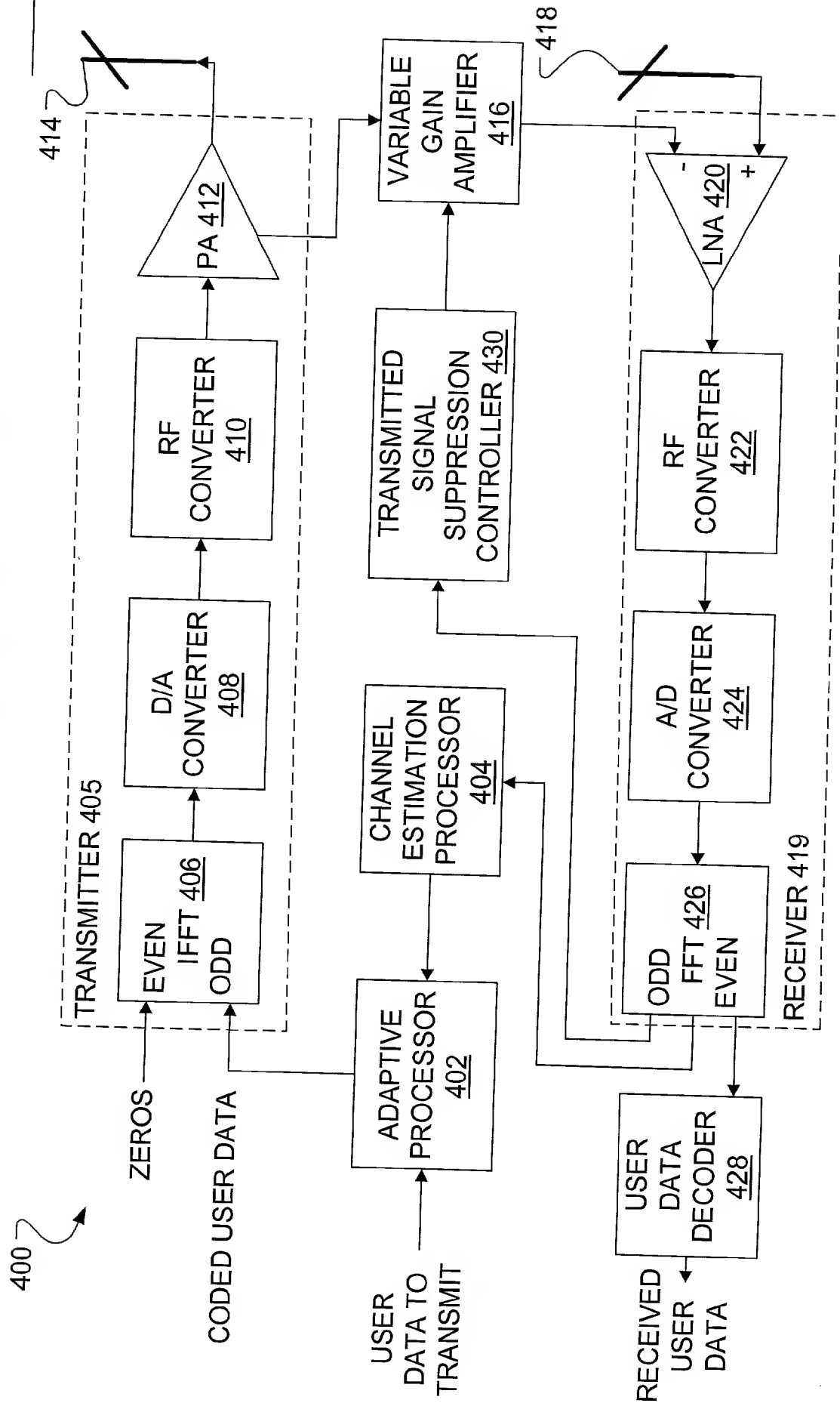


FIG. 4

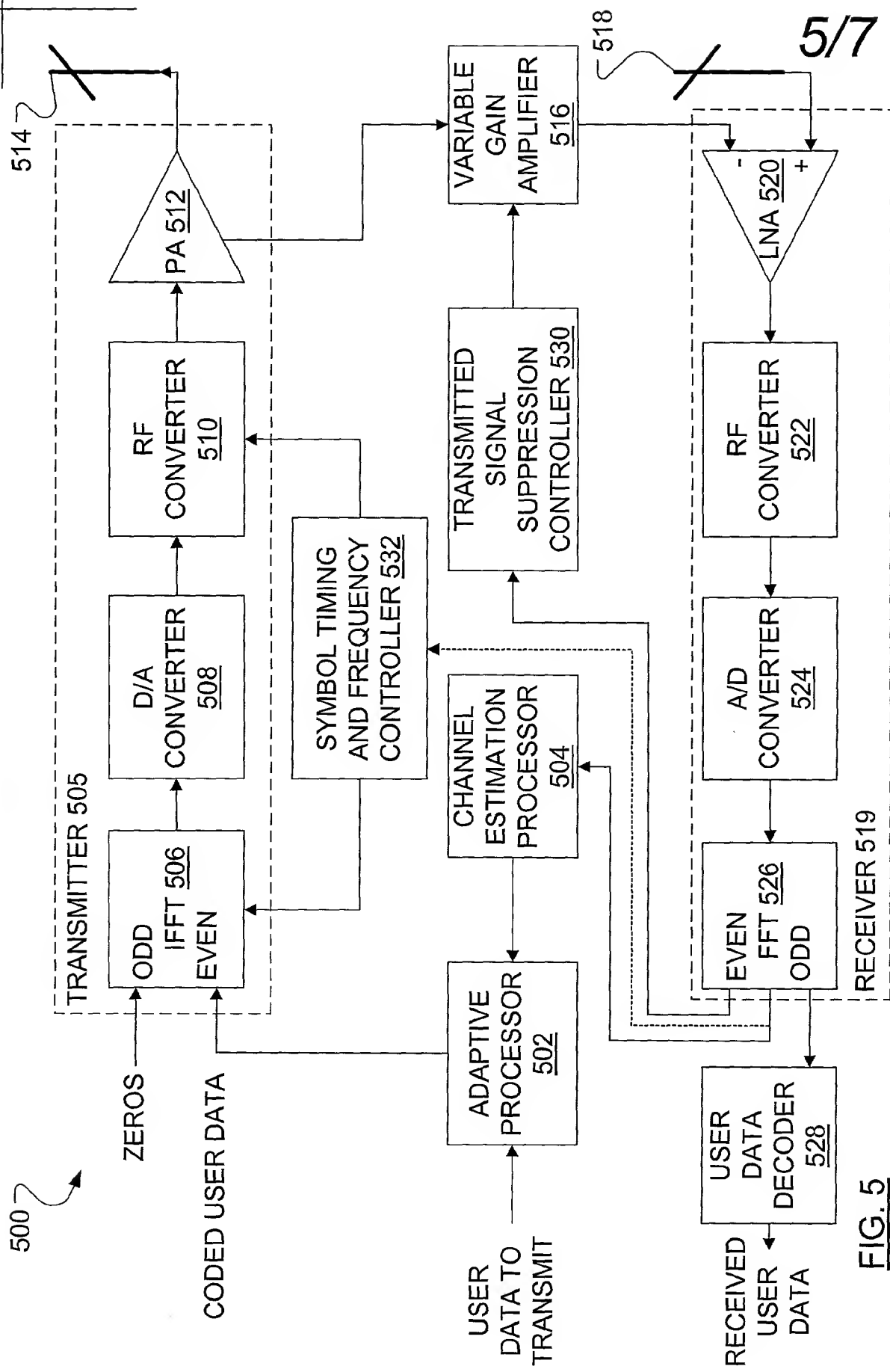


FIG. 5

FIG. 6 is a block diagram of a communication system 600, according to one embodiment of the present invention. The communication system 600 includes a transmitter 405 and a receiver 419. The transmitter 405 includes an even IFFT block 406, a D/A converter block 408, an RF converter block 410, and a power amplifier block 412. The receiver 419 includes an LNA block 420, an RF converter block 422, an A/D converter block 424, and an odd FFT block 426. A channel estimation processor block 404 is connected to the transmitter 405 and the receiver 419. A transmitted signal suppression controller block 430 is connected to the transmitter 405 and the receiver 419. A variable gain amplifier block 416 is connected to the transmitter 405 and the receiver 419. An adaptive processor block 402 is connected to the transmitter 405 and the receiver 419. A user data decoder block 428 is connected to the receiver 419. An isolator block 634 is connected to the transmitter 405 and the receiver 419. A signal 636 is input to the transmitter 405. A signal 636 is output from the receiver 419. A signal 636 is input to the isolator block 634. A signal 636 is output from the isolator block 634. A signal 636 is input to the variable gain amplifier block 416. A signal 636 is output from the variable gain amplifier block 416. A signal 636 is input to the channel estimation processor block 404. A signal 636 is output from the channel estimation processor block 404. A signal 636 is input to the transmitted signal suppression controller block 430. A signal 636 is output from the transmitted signal suppression controller block 430. A signal 636 is input to the adaptive processor block 402. A signal 636 is output from the adaptive processor block 402. A signal 636 is input to the user data decoder block 428. A signal 636 is output from the user data decoder block 428.

600

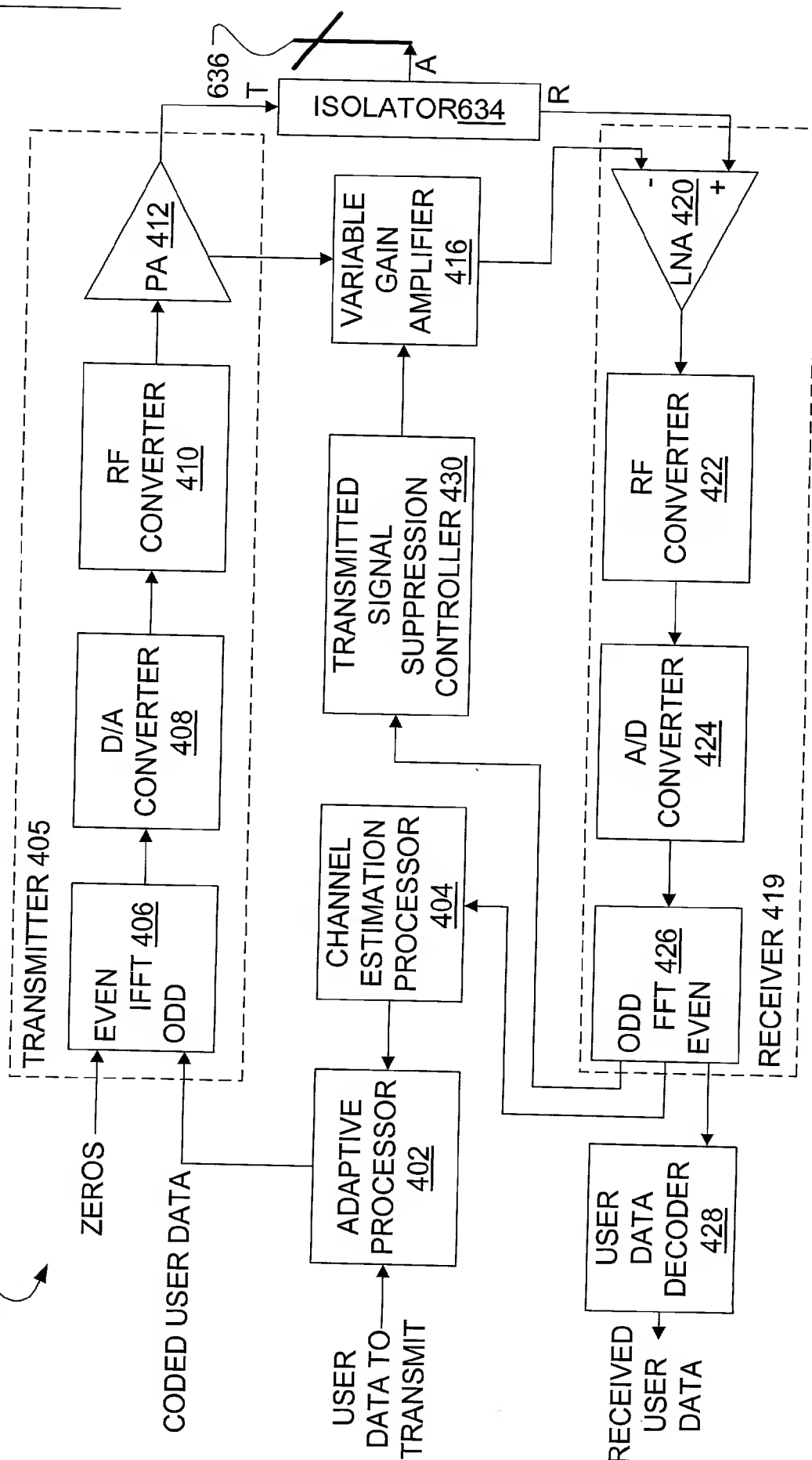


FIG. 6

700

Fig. 7 is a block diagram of a communication system 700, in accordance with an embodiment of the present invention. The communication system 700 includes a transmitter 505 and a receiver 519. The transmitter 505 includes an odd IFFT block 506, a D/A converter 508, an RF converter 510, and a power amplifier 512. The receiver 519 includes an LNA 520, an RF converter 522, an A/D converter 524, an even FFT block 526, and a user data decoder 528. A channel estimation processor 504 and a transmitted signal suppression controller 530 are connected to both the transmitter 505 and the receiver 519. An adaptive processor 502 is connected to the transmitter 505 and the receiver 519. A symbol timing and frequency controller 532 is connected to the transmitter 505. A variable gain amplifier 516 is connected to the transmitter 505 and the receiver 519. An isolator 734 is connected to the transmitter 505 and the receiver 519. A signal 736 is input to the transmitter 505 and the receiver 519. The transmitter 505 and receiver 519 are connected to an antenna 736 via an isolator 734. The transmitter 505 and receiver 519 are connected to a channel estimation processor 504 and a transmitted signal suppression controller 530. An adaptive processor 502 is connected to the transmitter 505 and the receiver 519. A symbol timing and frequency controller 532 is connected to the transmitter 505. A variable gain amplifier 516 is connected to the transmitter 505 and the receiver 519. An isolator 734 is connected to the transmitter 505 and the receiver 519. A signal 736 is input to the transmitter 505 and the receiver 519.

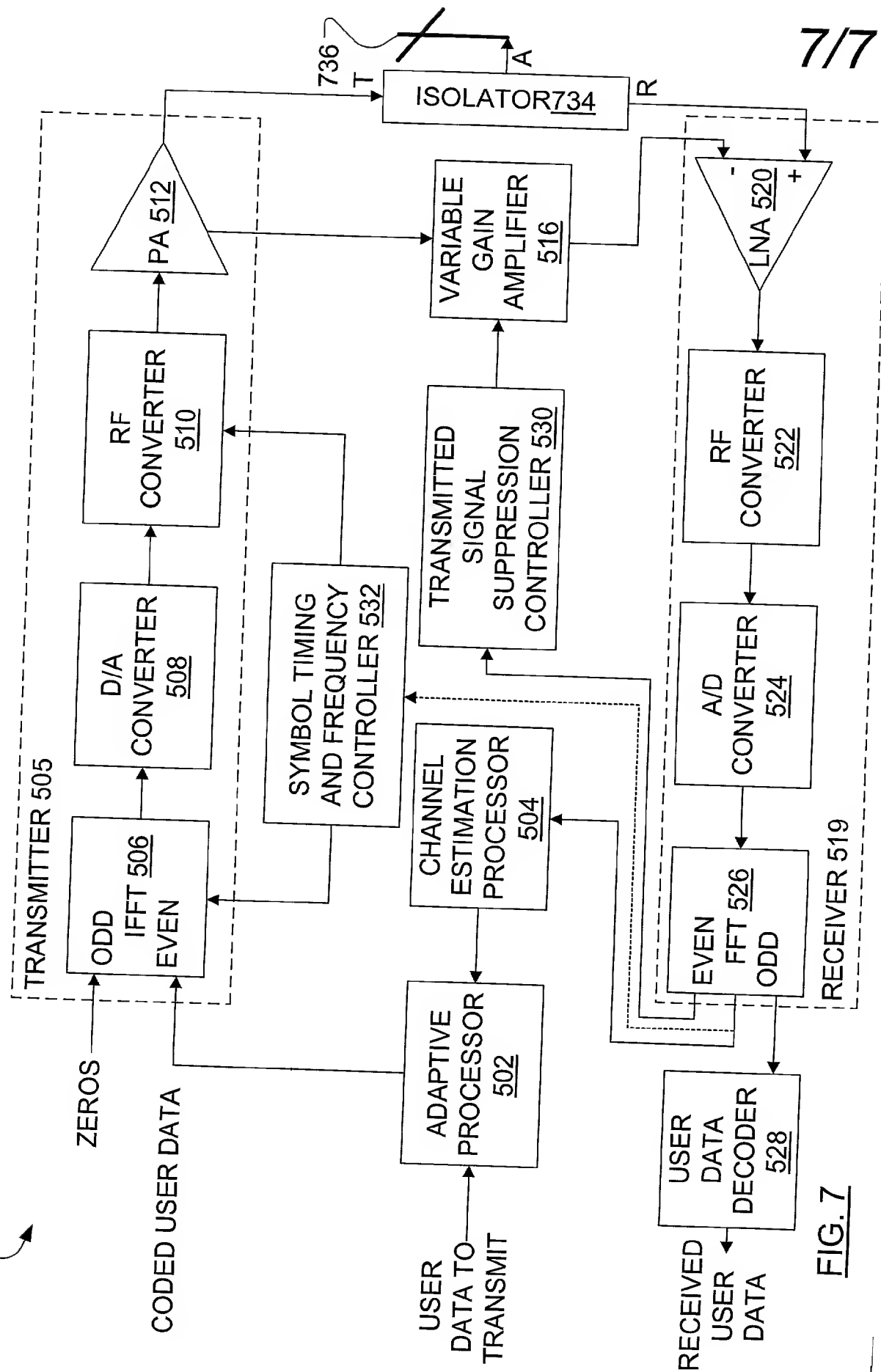


FIG. 7